GROUP PROJECT 1

OBJECTIVES:

1. Engage the student in cooperative thinking and problem solving.
2. Expose the CET 3116 student to the new Digital Programmable Devices technology such as Read Only Memories (ROM), Programmable Logic Arrays (PLA), Complex Programmable Device (CPLD) and Field Programmable Gate Array (FPGA).
3. Provide the CET 3116 student with the opportunity of familiarize with the modern methodologies of Digital Design and the Automated Digital Design Environment.
4. Analyze and compare different alternatives of automated tools for design, simulation, implementation and testing of Digital Systems available in the market.

DESCRIPTION

Each group will do a research and produce formal written report and a presentation that include at least the following topics:

1. Digital Programmable Devices technology.
2. FPGA Design Flow.
3. Automated tools for design, simulation, and implementation and testing of Digital Systems.

GUIDELINES:

1. This Group Project will account of 33% of the lab-project grade.
2. Each group will be selected randomly.
3. The group will have a discussion board created for interchanging ideas and communication between the members of the group and with the instructor. Other tools, such as chat room and white board, may be added later.
    - Posting should demonstrate knowledge of the subject and a professional approach to the solution of issues that may arise during the research.
4. Each member of the group will be evaluated by the rest of the members (peer evaluation).
5. Each member individually, will prepare an essay before the groups are structured. The essay should demonstrate that each member of the group has acquired basic knowledge of the matter to be treated in the project. The essay will count for 25% of the grade.
6. The group will research and report the referred topics based in the following:
    - Accomplishing the objectives established above.
    - Technological and economic benefits of the technology analyzed.
    - Relevance of the research with the CET 3116 course. The level of detail should be kept within the CET 3116 scope.
7. The group will write a report with the result of the analysis.
    - The report should not exceed 10 pages.
    - The report should contain an abstract, and a list of references.
    - Reports should follow the IEEE format.
    - Only one report per group will be turned in.

8. Each group will produce a power point presentation, with a maximum of 12 slides describing each group results.
    - Each presentation will be available to the rest of the course through Florida Online.
    - The presentation should address the most relevant points of the research.
9. There are many sources of information available to search for the case study:
    - A tutorial that covers FPGA and CPLDs is available in the drop box of this project. Though it is a bit old, it makes a good introductory document.
    - The Textbook and reference books given in the Syllabus have some of the topics covered in detail.
    - Providers of FPGAs like Altera Corp and XILINX have free automated tools, tutorials and documentation available to students and teachers.
    - We encourage the review of Quartus II from Altera Corp., since we will be using it in the subsequent labs.
10. The project will be evaluated considering the following aspects:
    - A rubric to evaluate the project is available in the project section. Special attention will be given to the following aspects:
        i. Project preparation: initial research and choices for case study.
        ii. Team preparedness to approach GroupWise activities. Each member of the group must be prepared (read and know the material) before planning.
        iii. Group management and communication of ideas within the group.
        iv. Quality, coherence and level of the Report and Presentation.
11. More guidelines will be posted as the project progress.
12. **Deadlines:**
    - Individual essay submitted by Sunday March 1st 11:59 p.m.
    - Written Report and presentation due Sunday March 22nd